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09/922,742	08/07/2001	Toshikazu Nakamura	108066-00038	9593

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EXAMINER
VITAL, PIERRE M

ART UNIT	PAPER NUMBER
2188	4

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/922,742	NAKAMURA, TOSHIKAZU	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,8-13 and 15-20* is/are rejected.

7)☐ Claim(s) *2,3,6,7 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement filed August 7, 2001 complies with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

3. The disclosure is objected to because of the following informalities:

The first occurrence of all acronyms should be defined to enable complete illustration and understanding of the claimed invention. As such, the term "LSI" is not properly defined as required for acronyms. Acronyms must be defined at their first usage in the disclosure. The entire disclosure should be checked for the proper use of acronyms.

Appropriate correction is required.

Claim Objections

4. Claim 10 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. It is improper under 35 U.S.C. 112 and 37 CFR 1.75(c) to have a dependent claim depending from a multiple dependent claim.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 16-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 recites the limitation "said clock buffer controller are provided" in line 2 and "each said clock buffer controller" in line 4 of the claim. Only "one clock buffer controller" was previously mentioned in independent claim 15.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 12, 13 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Kanazashi et al (US6,337,833).

As per claims 12 and 19, Kanazashi discloses a semiconductor integrated circuit that fetches input signals in synchronization with an internal clock signal generated by a clock buffer [*input buffer 54 fetches external clock CLK and generates internal clock signal I-CLK;* col. 4, lines 9-12; *input buffer inputs supplied address signals synchronized with the clock;* col. 2, lines 30-31]; comprising a clock buffer controller that activates said clock buffer only when there is a change in said input signals [*when read command is detected, clock supply control signal generates clock supply control signals Readz, Redcz;* col. 1, lines 27-33; col. 5, lines 55-67].

As per claim 13, Kanazashi discloses an input buffer that generates an internal signal from said input signal in synchronization with said internal clock signal [*input buffer inputs data and address signals synchronized with the internal clock signals;* col. 1, lines 34-37].

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakurai (US6,064,627) and Kanazashi et al (US6,337,833).

As per claims 15 and 20, Sakurai a semiconductor integrated circuit comprising a plurality of input buffers that fetches input signals in synchronization with an internal clock signal generated by a clock buffer [col. 2, lines 25-36].

However, Sakurai does not specifically teach a clock buffer controller that activates said clock buffer only when there is a change in said input signal in at least one of said input buffers [*when read command is detected, clock supply control signal generates clock supply control signals Readz, Redcz;* col. 1, lines 27-33; col. 5, lines 55-67].

Kanazashi discloses a clock buffer controller that activates said clock buffer only when there is a change in said input signal in at least one of said input buffers [*when read command is detected, clock supply control signal generates clock supply control signals Readz, Redcz;* col. 1, lines 27-33; col. 5, lines 55-67].

It would have been obvious to one of ordinary skill in the art, having the teachings of Sakurai and Kanazashi before him at the time the invention was made, to modify the system of Sakurai to include a clock buffer controller that activates said clock buffer only when there is a change in said input signal in at least one of said input

buffers because it would have reduced current consumption by reducing the number of clock signals supply actions that require large current drive [col. 2, lines 26-27] as taught by Kanazashi.

11. Claims 1, 5, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazashi et al (US6,337,833) and Uchida (US6,188,641).

As per claims 1, 5 and 11, Kanazashi discloses a synchronous dynamic memory operating in synchronization with an external clock [col. 1, lines 11-12] comprising a clock input buffer receiving said external clock and outputting an internal clock [*input buffer 54 fetches external clock CLK and generates internal clock signal I-CLK;* col. 4, lines 9-12]; an address input buffer receiving addresses in synchronization with said internal clock [*input buffer inputs supplied address signals synchronized with the clock;* col. 2, lines 30-31]; a data input buffer receiving data in synchronization with said internal clock [*input buffer inputs supplied data signals synchronized with the clock;* col. 2, lines 30-31]; wherein said clock input buffer supplies said internal clock to said command, address and data input buffers in normal operation mode [*in non-power-down-state, internal clock signal I-CLK is supplied continuously to the internal data read circuit 30 and address buffer 14, etc.;* col. 7, lines 43-48]; and wherein said clock input buffer supplies said internal clock to said command input buffer and stops supply of said internal clock to said address input buffer or data input buffer in data hold mode [*in power down state no clock signal is supplied to the internal circuitry which includes input buffer for inputting data and address signals;* col. 4, lines 39-42, col. 1, lines 34-41].

However, even though Kanazashi discloses the use of a command decoder, the reference fails to specifically teach a command input buffer receiving commands in synchronization with said internal clock.

Uchida discloses the use of a command decoder, the reference fails to specifically teach a command input buffer receiving commands in synchronization with said internal clock [col. 2, lines 1-4].

It would have been obvious to one of ordinary skill in the art, having the teachings of Kanazashi and Uchida before him at the time the invention was made, to modify the system of Kanazashi to include the use of a command decoder, the reference fails to specifically teach a command input buffer receiving commands in synchronization with said internal clock because it would have realized a higher speed of system by increasing the time allocated for providing commands to a chip to which access is desired as taught by Uchida [col. 12, lines 62-64].

12. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazashi et al (US6,337,833) and Uchida (US6,188,641) and further in view of Yada et al. (US6,266,294).

As per claims 4 and 8, the combination of Kanazashi and Uchida discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Kanazashi and Uchida fails to specifically teach a clock input buffer receiving a clock enable signal that distinguishes between normal operation mode and

power down mode, and said data hold mode includes this power down mode as recited in the claims.

Yada discloses a clock input buffer receiving a clock enable signal that distinguishes between normal operation mode and power down mode, and said data hold mode includes this power down mode [*clock enable signal goes to level L to shift to low power consumption mode and halt operation of the address buffer;* col. 4, lines 49-56; col. 5, lines 10-13].

It would have been obvious to one of ordinary skill in the art, having the teachings of Kanazashi and Uchida and Yada before him at the time the invention was made, to modify the system of Kanazashi and Uchida to include a clock input buffer receiving a clock enable signal that distinguishes between normal operation mode and power down mode, and said data hold mode includes this power down mode because it would have improved the reliability of the SDRAM by allowing the internal clock signal to have an adequate pulse width so that the erroneous operation of the integrated circuit device is prevented [col. 3, lines 53-58] as taught by Yada.

13. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazashi et al (US6,337,833) and Uchida (US6,188,641) and further in view of Tomita et al (US6,272,069).

As per claims 9 and 10, the combination of Kanazashi and Uchida discloses the claimed invention as detailed above in the previous paragraphs. However, the

combination of Kanazashi and Uchida fails to specifically teach an LSI, wherein the synchronous dynamic memory is embedded on one chip with a processing circuit macro that implements a prescribed processing; and a memory controller that controls said synchronous dynamic memory as recited in the claims.

Tomita discloses an LSI, wherein the synchronous dynamic memory is embedded on one chip with a processing circuit macro that implements a prescribed processing [col. 1, lines 38-40]; and a memory controller that controls said synchronous dynamic memory [col. 1, lines 17-22].

It would have been obvious to one of ordinary skill in the art, having the teachings of Kanazashi and Uchida and Tomita before him at the time the invention was made, to modify the system of Kanazashi and Uchida to include an LSI, wherein the synchronous dynamic memory is embedded on one chip with a processing circuit macro that implements a prescribed processing; and a memory controller that controls said synchronous dynamic memory because it would have increased system performance by improving on the speed of data transfer between the logic section and the memory section [col. 1, lines 40-42] as taught by Tomita.

Allowable Subject Matter

14. Claims 2-3, 6-7 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record does not teach or suggest a clock input buffer driving a first and second clock supply lines in normal operation mode and said clock input buffer driving said first clock supply line and stops driving said second clock supply line in a data hold mode in combination with the other elements set forth in claims 2-3 and 6-7.

The prior art of record does not teach or suggest a clock buffer controller comparing an input signal with an internal signal output from an input buffer and activating said clock buffer when said input signal differs from said internal signal in combination with the other elements set forth in claim 14.

16. Claims 16-18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach SDRAM operating in synchronism with external clock, clock input buffer operating

in normal operation mode or data hold mode and activating clock buffer when there is change in input signal supplied to input buffer.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER

Pierre M. Vital
May 28, 2003